

# Barrier effect of capacitor

Are DRAM capacitors reaching the scaling limit?

DRAM capacitors are reaching the scaling limit and new approaches are necessary to enable further reduction of the physical thickness of the capacitor dielectric. The conduction band offset (CBO) of a platinum noble metal electrode on atomic layer deposited  $ZrO_2/Al_2O_3/ZrO_2$  is evaluated and compared to a titanium nitride electrode.

Does barrier height affect dielectric scaling?

The barrier height difference between the two electrodes is evaluated in comparison with a previously reported model. Finally, the impact of an increased barrier height on dielectric scaling will be discussed based on a leakage current simulation of a  $ZrO_2$  capacitor.

Is giant dielectric a grain boundary or a barrier layer capacitance?

The giant-dielectric phenomenon is therefore attributed to a grain boundary (internal) barrier layer capacitance (IBLC) instead of an intrinsic property associated with the crystal structure.

Does a top electrode deposition increase the thickness of the interfacial layer?

With this, we confirmed the above-discussed hypothesis that a top electrode deposition increases the thickness of the interfacial TiON layer at the bottom electrode by pulling out oxygen from the  $ZrO_2$  and creating vacancies in the dielectric close to the bottom electrode.

Does conduction band offset affect leakage current?

This leads to a decrease of the tunneling probability and the Poole-Frenkel current component. In addition, leakage current simulations showed that an increasing conduction band offset results in a decrease of the F-N tunneling leakage at high electric field.

How to scale down  $ZrO_2$  dielectric for future DRAM capacitors?

Therefore, conduction band offset improvements by introduction of inert metal electrodes with higher CBO represent one of the most effective ways to scale down the  $ZrO_2$  dielectric for future DRAM capacitors. Kil DS, Song HS, Lee KJ, Hong K, Kim JH, Park KS, et al. Proceedings of the symposium on VLSI technology digest of technical papers.

An internal barrier layer capacitor effect was observed in a 12R-type hexagonal perovskite  $Ba_4YMn_3O_{11.5}$  ceramic, which contains insulating grains and more resistive grain-boundary regions.

Introducing  $TiO_2$  as a barrier layer reduced the leakage current and EOT of Pt/BST/Si capacitor. The conduction mechanism in Pt/ $TiO_2$ /Si structure was found to be tunneling-like behaviour limited by the interfacial layer. Hysteresis could be minimized by the optimization of the annealing process. In reliability characteristics,  $TiO_2$  ...

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Electrical properties such as capacitance, dissipation factor, and insulation resistance are sensitive to plating process parameters used to deposit a nickel barrier layer and a tin/lead ...

A capacitor is an electrical component that stores energy in an electric field. It is a passive device that consists of two conductors separated by an insulating material known as a dielectric. When a voltage is applied across the conductors, an electric field develops across the dielectric, causing positive and negative charges to accumulate on the conductors.

Introducing TiO<sub>2</sub> as a barrier layer reduced the leakage current and EOT of Pt/BST/Si capacitor. The conduction mechanism in Pt/TiO<sub>2</sub>/Si structure was found to be tunneling ...

Also, we investigated the effect of various parameters of insulator materials as barrier layer such as effective mass of electron ( $m_e^*$ ), electron affinity ( $\chi$ ) and electron mobility ( $\mu$ ) on the performance of Pt/BST/Pt nanocapacitor. Even though enhancement in leakage current performance is observed while introducing barrier layers at Pt-BST interfaces in Pt/BST/Pt ...

In this paper, the effect of barrier layers in Pt/BT/Pt capacitors is studied using zinc oxide and aluminium oxide. The performance parameters such as capacitance density, leakage current, equivalent series resistance, dielectric loss and dielectric strength of Pt/BT/Pt thin film capacitors with barrier layers of different sizes are simulated ...

The d.c. conduction is investigated in the two different types of internal barrier layer capacitors, namely, (Mn, Nb)-doped SrTiO<sub>3</sub> (STO) and CaCu<sub>3</sub>Ti<sub>4</sub>O<sub>12</sub> (CCTO). Scanning electron microscopy (SEM) and Capacitance - Voltage (C-V) analysis are performed to estimate the effective electric field at a grain boundary,  $E_{GB}$ .

In this work the RTA effect on the TiN barrier for the Pt/BST/Pt/Ti/Si capacitors was investigated. By annealing the TiN barrier layer, good barrier properties, that is, displaying no serious inter-diffusion and under accurate RTA conditions were obtained. The RTA treatment at 600°C for 90 s improved the crystallinity of TiN and suppressed the ...

A new perovskite material Nd<sub>2</sub>/3CuTa<sub>4</sub>O<sub>12</sub> was applied as a naturally formed internal barrier layer capacitor. The powder prepared by solid state synthesis and ball milling was pressed into ...

This investigation reports the effect of rapid-thermal-annealing (RTA) on metallic barrier TiN against the interdiffusions of Ti and Si into barium strontium titanate (BST) in ...

CaCu<sub>3</sub>Ti<sub>4</sub>O<sub>12</sub> (CCTO) ceramics are potential candidates for capacitor applications due to their large dielectric permittivity ( $\epsilon''$ ) values of up to 300 000. The underlying mechanism for the high  $\epsilon''$ ...

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Electrical properties such as capacitance, dissipation factor, and insulation resistance are sensitive to plating process parameters used to deposit a nickel barrier layer and a tin/lead solder layer. The parameters in this study included: (1) three capacitor lots; (2) eight termination ink types; (3) seven termination bandwidths; (4) two ...

Semantic Scholar extracted view of "Effect of rapid-thermal-annealed TiN barrier layer on the Pt/BST/Pt capacitors prepared by RF magnetron co-sputter technique at low substrate temperature" by C. Hwang et al. Skip to search form Skip to main content Skip to account menu. Semantic Scholar's Logo. Search 221,086,391 papers from all fields of science. Search. Sign ...

This barrier layer electrical microstructure with effective permittivity values in excess of 10 000 can be fabricated by single-step processing in air at ~1100 °C.  $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$  is an attractive option to the currently used  $\text{BaTiO}_3$ -based materials which require complex, multistage processing routes to produce IBLCs of similar ...

This barrier layer electrical microstructure with effective permittivity values in excess of 10 000 can be fabricated by single-step processing in air at ~1100 °C.  $\text{CaCu}_3\text{Ti}_4\text{O}_{12}$  ...

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